Design of a Broad-Band 4-Bit Loaded Switched-Line Phase Shifter

GUY D. LYNES, GERALD E. JOHNSON, B. E. HUCKLEBERRY, AND NEIL H. FORREST

Abstract—**A 4-bit p-i-n diode switched-line phase shifter was fabricated for use in the 2.0- to 4.0-GHz frequency range. Extremely good phase characteristics were easily obtained over two octaves by employing a resistive loading technique to eliminate resonance problems. A single bit was modeled and analyzed on a computer from 1.5 to 6.0 GHz. Test results of a microstrip realization of this bit, which correlates well with the computer model, are presented. A unique compatible driver used with the phase shifter, and the microstrip fabrication process used in constructing the phase shifter are also presented.**

I. INTRODUCTION

FOUR types of diode phase shifters are generally well known: the switched line [1], [2], reflection [3], [4], loaded line [5], [6], and high pass low pass [7], [8]. Garver [9] presents an excellent discussion of these four common types of phase-shift circuits. According to Garver: "Although many versions of these phase shifters have been designed, none of the designs has exploited the full bandwidth possibilities of these circuits. Most designs to date have a maximum bandwidth of about 10 percent, but most of the circuits have a maximum potential bandwidth of an octave." Coats [10] has shown that an octave-band constant-phase (as a function of frequency) type of phase shifter can be constructed by using a shunt-mode switched-line type of phase shifter [11] with Schiffman sections [12]. The shunt-mode switch is not inherently broad band, however, since it depends on the shunt diodes being 1/4 wavelength from the switched junctions.

Historically, the bandwidths and maximum phase shifts of the switched line, reflection, and switched high-pass low-pass types of phase shifters have been limited by resonance effects which cause notches in the amplitude response and large errors in the phase response of these phase shifters. By eliminating the resonance effects, ultra-broad-band phase shifters with very large amounts of phase shift become possible.

Podell [13] has suggested a method of completely eliminating the undesired resonance effects in the switched-line type of phase shifter. By using two transfer switches in place of the two single-pole double-throw (SPDT) switches of the ordinary switched-line phase shifter the switched out line may be terminated on both ends in its characteristic impedance. Since the line is now properly terminated on both ends, no resonance can occur. Podell's technique effectively eliminates all of the undesired resonance effects. Elimination of the resonance effects makes it possible to construct multioctave phase shifters with virtually any desired amount of phase shift. With the resonance problems removed, the only limitations to bandwidth and the amount of phase shift are the RF properties of the diodes, and the dc bias circuits. An interesting technique for using ferrite loading to reduce the resonance effects was presented by Sato and Naito [14] and Kosugi, Naito, and Sawada [15]. Several methods of using resistive loading to eliminate resonance effects in switched line, reflection, and high-pass low-pass phase shifters were presented by Lynes [16].

This paper addresses the design of a 4-bit phase shifter of the switched-line type using a resistive loading technique to avoid resonance problems. It presents the results of a computer analysis and the experimental verification of a single bit of a 4-bit phase shifter, and experimental results only for a complete 4-bit phase shifter. In addition, a unique driver circuit and the construction techniques used to fabricate the 4-bit phase shifter are discussed.

II. SWITCHED-LINE PHASE-SHIFTER DESIGN AND ANALYSIS

A. Resistively Loaded Switched-Line Phase Shifter

The ordinary type of switched-line phase shifter [shown in Fig. 1(a)] is based on a very simple concept. Essentially, this type phase shifter is comprised of two SPDT switches, and two transmission lines of different lengths. By al-

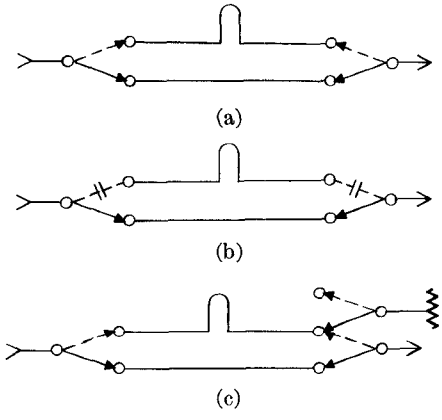

Fig. 1. The switched-line type of phase shifter. (a) The basic circuit. (b) An equivalent circuit. (c) One method of avoiding resonance problems.

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ternately switching the transmission lines this phase shifter yields a time delay that is independent of frequency, and a phase shift that is a linear function of the frequency. This type of phase response is ideal for phased-array applications (if used as a true time delay element). However, this simple version of a switched-line phase shifter has a serious problem. When either of the two lines has an electrical length of $\frac{1}{2}$ wavelength, or an integral number of half wavelengths, it forms a high Q resonator when it is the "switched out" line. The open contacts of the p-i-n diode switches are lightly coupled to this resonant line, as shown in the equivalent circuit for the switched-line phase shifter in Fig. 1(b). This coupling to the resonant line causes a sharp insertion loss notch in amplitude response at the resonant frequency, and large phase errors near resonance.

One method for eliminating these resonance problems is shown in Fig. 1(c). If the short path is made short enough, the first resonant frequency occurs above the highest frequency of interest. By loading one end of the potentially resonant long path in its characteristic impedance, the line no longer has a natural resonant frequency. Some power will, of course, still be coupled to the long path when it is the "switched out" path. Since the line is no longer resonant, however, the amount of power coupled over will be minimal. Since the main transmission path, i.e., the short path, is capacitively coupled to the singly terminated line at two points, it can be expected that the amount of power lost to the termination will be a function of the electrical lengths between the coupling points, and the value of the junction capacitance of the diodes. Some phase error can also be expected from this coupling.

B. Computer Analysis

A brief computer analysis was performed to confirm the statements made in the preceding discussion, and also to determine the performance constraints over a wide bandwidth. Fig. 2(a) shows the single-bit model used in this analysis. The sections labeled l_1, l_2, and l_3 represent transmission line lengths. The diode equivalent circuit is shown in Fig. 2(b). Assuming the use of a series chip p-i-n diode, L_s represents the series inductance of the wire bond used to attach the diode, R_s is the diode series resistance, R_j is the junction resistance, C_j is the junction capacitance, and C_g is the capacitance of the gap across which the diode is attached.

The analysis was performed using conventional node-voltage equations, modified to incorporate the transmission line equations. An admittance matrix was then determined, inverted, and multiplied by the assumed input current. The resulting node voltages were then converted to conventional microwave parameters, i.e., insertion loss, return loss, and phase.

The analysis is based on using a microstrip transmission line on a 0.025-in alumina (99.5 percent) substrate with a dielectric constant of 9.8. The diodes are HP 5082-0012 p-i-n diode chips. The program assumes a TEM transmission mode for the microstrip, with a complex propagation constant. The attenuation constant was assumed to be

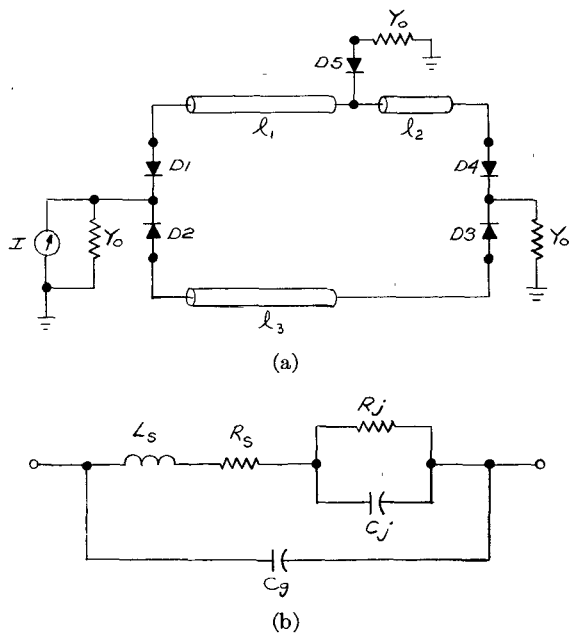

Fig. 2. Models used for computer analysis. (a) Loaded switched-line phase-shifter model. (b) Diode model.

$$\alpha = 0.07 \quad (f_{\mathrm{GHz}})^{1/2} \text{ dB/in}$$

with the effective dielectric constant assumed to be 6.56.

Table I lists the parameters used in the analysis. The gap capacitance (C_g) is assumed to be 0.015 pF, which corresponds to a 10-mil gap. The junction resistance is varied from 0 to 8000 Ω to simulate the two diode states. The lengths shown in this example yield a phase shift of 45° at 2.0 GHz.

The results of the analysis, from 1.5 to 6.0 GHz, are shown in Figs. 3–5. The computations were made with and without loading the long path. The computed phase shift is shown in Fig. 3. The phase deviation due to the resonance of the long path is shown as a dashed curve. When the long path is loaded, the straight solid line phase response is obtained. This straight line, however, is not quite ideal. If a perfectly straight line were drawn through the end points, i.e., at 1.5 and 6.0 GHz, a deviation of less than 0.5° would occur at the center frequency (3.75 GHz). Ideally, the slope of the straight line response of the phase shifter would be such that an extrapolation of the phase response back to zero frequency would pass through the origin. An extrapolation of the straight line passing through the end points of the computed response misses the origin by less than 1°.

The calculated effect of the load on the insertion loss of the long path is shown in Fig. 4. In the unloaded case, the 50-Ω load is completely removed from the circuit. In the loaded case, the 50-Ω load is in the circuit but the diode coupling it to the long line is back biased. The additional insertion loss in the loaded case, therefore, is due to the finite isolation of the diode. Since the diode impedance is

TABLE I
PARAMETERS USED IN THE ANALYSIS

Circuit Parameters	Diode Parameters
l_1: 0.538 in	L_s: 0.3 nH
l_2: 0.050 in	R_s: 0.8 Ω
l_3: 0.300 in	R_j: 0, 8000 Ω
Y_0: 0.02 mhos	C_j: 0.07 pF
	C_d: 0.015 pF

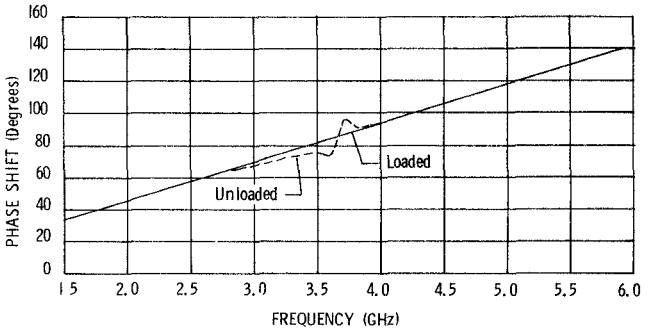

Fig. 3. Calculated phase response of a single-phase bit with and without resistive loading.

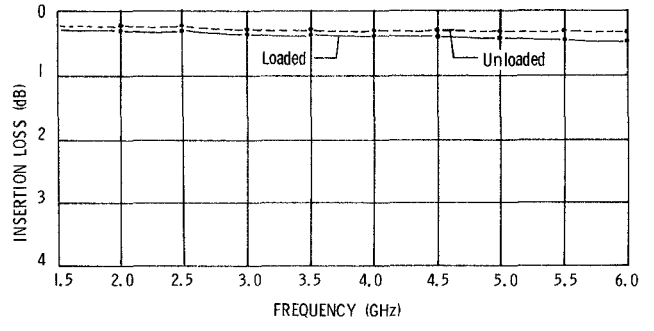

Fig. 4. Calculated amplitude response of a single-phase bit in the maximum phase delay state (long path) with and without the resistive loading circuitry.

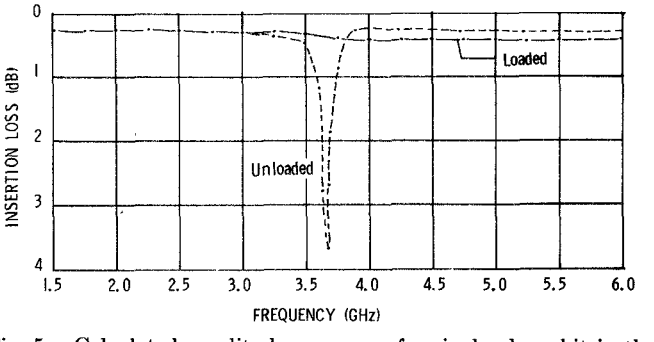

Fig. 5. Calculated amplitude response of a single-phase bit in the minimum phase delay state (short path) with and without the resistive loading circuitry.

basically capactive, it is not surprising to see the additional loss (in the loaded circuit) increase as a function of frequency.

The calculated effect of the load on the insertion loss of the short path is shown in Fig. 5. The amplitude notch due to resonance of the "switched out" long path is clearly visible in the unloaded case. When one end of the long path is loaded in its characteristic impedance the notch is no longer present.

C. Driver Considerations

The driver circuits required to bias the p-i-n diodes in the phase shifters initially presented a problem, but its solution was unique and simple. It is common design practice for a microwave engineer to develop a phase-shifter circuit and specify the driver requirements for a circuit designer to comply with. This method usually leads to a circuit design that is overly complicated. This produces exessive material, packaging, and assembly costs that are very undesirable for a multielement array.

Our approach was to develop the driver circuit and the microwave circuit concurrently. This optimizes the use of thin film and integrated circuit technology, consequently reducing the component count, size, voltage requirements, power requirements and, primarily, reduces cost. This method resulted in a very simple circuit that can be driven directly from TTL logic levels. All drive requirements for each 4-bit phase shifter are supplied by two SN74128 TTL circuits. A schematic diagram of this bias circuit is shown in Fig. 6.

Referring to Fig. 6, when bit 1 is in the minimum phase state, $A3$ is high and $A2$ is low. The high signal level (approximately 3.5 V) at filtercon $F2$ produces a current flow in diodes $D2$ and $D3$ which switches them to their low impedance states and produces a voltage drop across resistors $R1$ and $R2$. Since $A2$ is holding the voltage low (0 V) at $F1$, diodes $D1$ and $D4$ are back biased. This disconnects the maximum phase line from the circuit, except where it is resonant. This problem is solved by loading the line with 50 Ω through diode $D5$. The low voltage at $F1$ causes a current to flow through diode $D5$, which produces a low impedance state.

When the maximum phase state is desired, the voltages are reversed at $F1$ and $F2$ by drivers $A2$ and $A3$. This produces a current in diodes $D1$ and $D4$, maintaining the volt drop across resistors $R1$ and $R2$. Diodes $D2$ and $D3$ are thereby reverse biased by virtue of the low at $F2$. Diode $D5$ is also reverse biased since the voltage divider maintains a small (< 2.5 V) positive voltage at the junction.

All resistors external to the SN74128 drivers are thin-film resistors, deposited directly on the microwave substate. For our purposes, the SN74128's were mounted on small PC boards, which in turn were mounted directly on each phase-shifter module.

The switching speed of the driver circuit is approximately 300 ns. This value is limited by the filtercons ($F1$, $F2$, etc.), but for most phased-array applications it is quite adequate. If more speed is desired, the SN74128 drivers must be placed inside the phase-shift modules.

D. Fabrication

The phase shifters were built on an alumina or aluminum oxide substrate. The alumina substrates used are 99.5

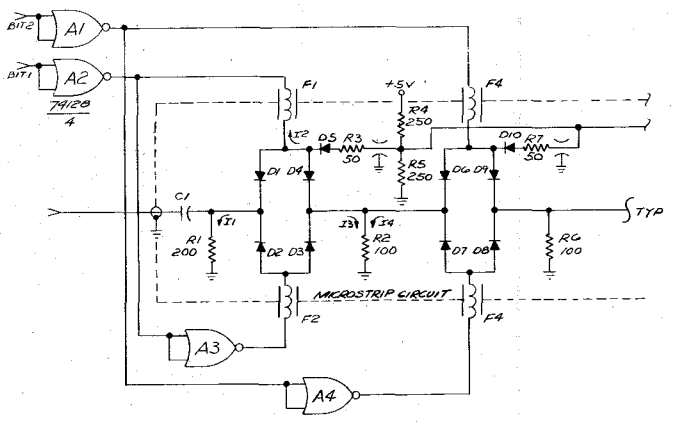

Fig. 6. Phase-shifter bias schematic.

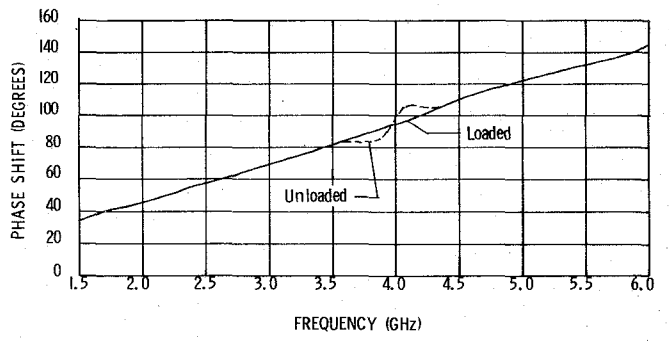

Fig. 7. Measured phase response of a single-phase bit with and without resistive loading.

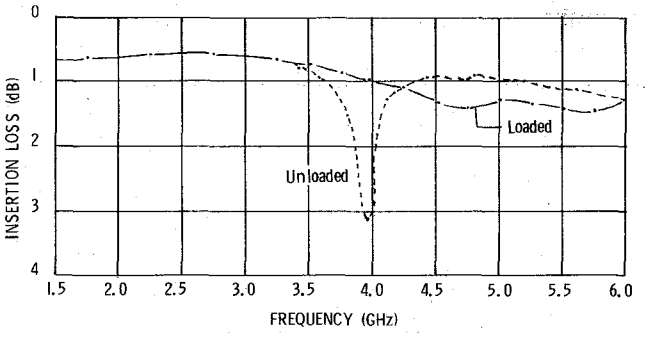

Fig. 8. Measured amplitude response of a single-phase bit in the minimum phase delay state (short path) with and without resistive loading.

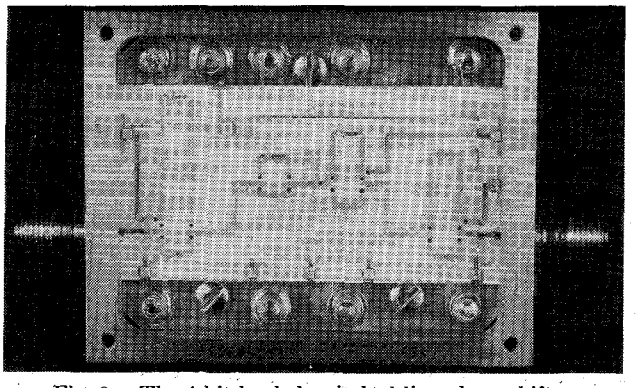

Fig. 9. The 4-bit loaded switched-line phase shifter.

percent pure Al_2O_3 and have an "as fired" surface finish of 4 μin CLA, or better.

The fabrication technique used for the phase shifter utilized NiCr–Au for the resistor–conductor layers. The NiCr forms the adhesive layer for the gold, as well as the resistive layer. The NiCr is deposited to a nominal 80 Ω per square, which results in a final value of 100 Ω per square, and a TCR of +20 parts per million/°C.

The assembly techniques used to fabricate the phase shifter do not differ significantly from those used for hybrid microcircuit assembly. The p-i-n diodes were eutectically die bonded to the plated gold conductors, the MOS beam lead capacitors were attached utilizing a commercial beam lead bonder, and all the internal bonding, including that for the p-i-n diode, was performed with a thermocompression bonder fitted with 1-mil gold wire. Connections from the circuit to the bias terminals were welded using a split-tip parallel gap welder and 2-mil gold wire.

E. Experimental Data

1) Single-Bit Test Results: An experimental model of a single bit was fabricated and tested to obtain confirmation of the computer analysis results. The long path was loaded external to the circuit so that more detailed measurements of the circuit operation could be made. The experimental circuit was built in the form shown in Fig. 2(a), except for the addition of RF bias chokes. The physical layout of this phase-shifter bit is identical to the third bit from the left in Fig. 9.

The measured phase and amplitude response of this bit are shown in Figs. 7 and 8, respectively. The unloaded data was obtained by back biasing the loading diode to disconnect the 50-Ω termination. This is slightly different from the computer model, where all the loading circuitry was completely removed. The phase response for both the loaded and unloaded conditions is shown in Fig. 7. The linearity of the phase (about ±2°) in the loaded case is quite good. The insertion loss through the short path with and without loading is shown in Fig. 8. The effects of the resonance on the "switched out" long line can be clearly seen in both the amplitude and the phase response of the phase shifter.

Note that there is very close agreement between the measured data shown in Figs. 7 and 8 and the calculated data shown in Figs. 3 and 5. There are some minor observable differences however. The computed data shows an overall higher Q (as seen by the lower average insertion loss), and greater depth to the resonance. The measured data show the resonance occurring at a slightly higher frequency than computed. This is the result of an approximation in estimating the electrical length of the long path.

2) The 4-Bit Phase Shifter: A 4-bit phase shifter in the 2.0–4.0-GHz range was designed using the loaded switched-line technique. This phase shifter was designed for use in a modulo 2π system which operates from 2.0 to 4.0 GHz. Therefore, at 2.0 GHz the design phase-bit values are 22.5°, 45°, 90°, and 180°.

The 4-bit phase shifter is shown in Fig. 9. All of the short paths are short enough so that their resonant frequencies occur above 4 GHz. Therefore, none of the short paths are loaded. The resonance associated with the long

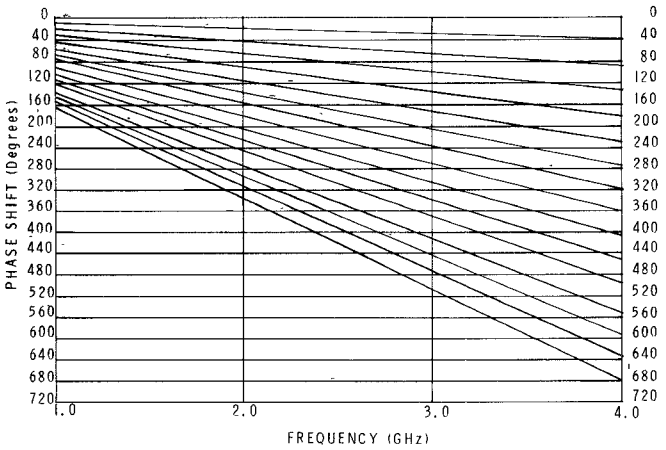

Fig. 10. Measured phase response of all states of the 4-bit phase shifter.

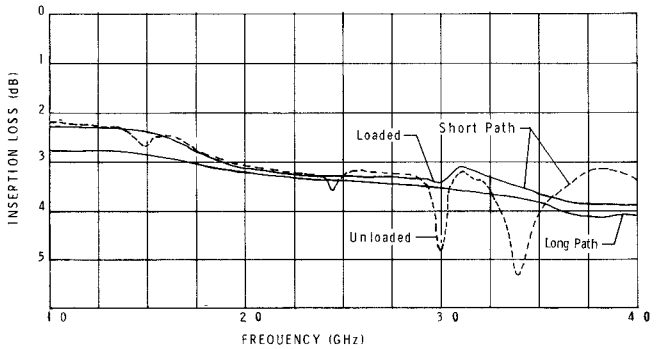

Fig. 11. Measured amplitude response of the 4-bit phase shitter in the maximum (long path) phase state with loading and the minimum (short path) phase state with and without loading.

path in the smallest phase bit also occurs above 4 GHz so it is not loaded. Each of the other three long paths have resonant frequencies in the 2.0–4.0-GHz band and, therefore, are each loaded at one end. It should be noted that due to the symmetry of the circuits the absolute path lengths are unimportant to the phase response; only the difference in path length is critical. This makes the path length computations straightforward. The 50-Ω loading resistors and the bias resistors are all thin-film components, included on the substrate. The RF bias chokes consist of 18 turns of 0.002-in wire, going either to a bypassed bias resistor, or to a filtercon passing through the package to the driver circuit mounted at the rear of the package. RF grounds for the 50-Ω terminations are obtained via a small ground plane on the top side of the substrate, which is clamped under the edge of the circuit frame. The narrow conductor on the upper part of the substrate is the +5-V bias line.

The test results for the experimental 4-bit phase shifter from 1.0 to 4.0 GHz are shown in Figs. 10 and 11. Fig. 10 shows the total phase response, including all the composite bit positions ($2^4 = 16$). The total ideal accumulated phase for the four bits should be 168.75° at 1 GHz, 337.5° at 2.0 GHz, and 675° at 4.0 GHz.

As was the case with the simple single-test bit, the phase is very close at 1.0 and 2.0 GHz, and slightly high at 4.0 GHz (by about 5°). Excellent phase linearity was obtained in all bit positions (better than ±2.5°).

Fig. 11 shows the insertion loss for three different conditions: short path loaded, long path loaded, and short path unloaded. The unloaded data shows four different resonances which would cause serious degradations in both the phase and amplitude response, without loading. The "short path loaded" and the "long path loaded" curves form an envelope which encompasses the insertion losses of all the states. The measured VSWR was less than 1.7:1 in all bias states from 1.0 to 4.0 GHz.

III. CONCLUSIONS

A practical 4-bit time-delay type phase shifter was built for modulo 2π operation from 2 to 4 GHz. It was shown that by employing the resistive loading technique the bandwidth and "amount of phase-shift" limitations of switched-line phase shifters are removed. This technique should prove to be very useful in the construction of very broad-band phase shifters of both the time-delay and constant-phase-shift types.

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